REMARKS

1. Applicant has amended the specification at the following places to correct informalities noted by applicant's attorney upon a further study of the specification.

Page 8, line 8,

Page 8, line 9,

Page 12, line 15,

Applicant respectfully submits that these changes are supported by the application as originally filed.

2. The Examiner has objected to the drawings on the basis that the drawings do not designate "the first electrical conductor" and "the second electrical conductor." Applicant respectfully disagrees with the position of the Examiner. Each of the plate 32 and the ring 30 has been identified as an "electrical conductor" in the application as originally filed. The designation of the plate 32 and the ring 30 as "electrical conductors" in the drawings is accordingly extraneous. Applicant has amended the specification on page 8, line 10, of the specification in the previous amendment to indicate that the plate 30 and the ring 32 may be considered as electrical conductors and the Examiner has accepted this addition to the specification. This should be sufficient to teach a person of ordinary skill in the art.

In order to avoid a controversy with the Examiner, applicant has amended the drawings to indicate that the ring 32 constitutes an electrical conductor and the plate 30 constitutes an electrical conductor. Applicant has also amended the specification to

indicate that the ring 32 constitutes one electrical conductor and the plate 30 constitutes another electrical conductor.

3. Applicant confirms that he has made a provisional election with traverse to prosecute the invention of group I, claims 1-21, and that claims 22-42 are withdrawn from consideration in this application. Claims 43-51 were added by an amendment dated December 3, 2002. Applicant respectfully submits that claims 43-51 are properly in this application and that they should be prosecuted with claims 1-21.

4. Claims 1-4, 7-9, 11, 14-16, 19-21, 43-47 and 50 have been rejected under 35 U.S.C. 102(b) as being anticipated by Koshimizu and "demonstrated" by Mountsier. The rejection by the Examiner is improper because Koshimizu and Mountsier do not teach what the Examiner says that they teach.

According to the Examiner on page 4 of the Office Action dated 02/13/2003, Koshimizu teaches that electrodes 116 and 110 are biased to different voltages. This is not true. The electrodes 116 and 110 are biased to the same voltage. This may be seen from the following statement by Koshimizu in column 4, lines 48-50.

> "...preferably the same high frequency power is, (sic) applied to the first and second susceptors 110 and 116, respectively."

The Examiner appears to be interpreting Koshimizu on the basis that the susceptors 110 and 116 appear to be operating on a single wafer W. This is not true. The susceptor 116 appears to be operating independently on a second wafer. This may be seen from the following statement in column 6, lines 27-31 of Koshimizu.

> "Moreover, in the etching apparatus 100, wafers W fixed on the first and second susceptors 110 and 116 can

simultaneously be subjected to the same etching process, thereby increasing the throughput of the apparatus." (underlining supplied)

This sentence not only confirms that the susceptors 110 and 116 operate independently of each other to process separate wafers W but it also confirms that the susceptors 110 and 116 receive the same power. Since the susceptors 110 and 116 in Koshimizu receive the same power and operate independently of each other, they cannot be considered as equivalent to the electrodes 22 and 24 in applicants invention.

Koshimizu also does not disclose that the alternating voltage from the source 134 provides a DC bias on the susceptor 116 or that the alternating voltage from the source 130 provides a DC bias on the susceptor 110. If the Examiner still believes that the alternating voltage sources 130 and 132 provide DC biases respectively on the susceptors 110 and 116, applicant would appreciate it if the Examiner would specify in the next Office Action where Koshimizu discloses this. Actually, Mountsier also does not disclose this. Applicant would accordingly appreciate it if the Examiner would specify in the next Office Action where Mountsier discloses this.

The Examiner has indicated that the members 104 and 204 in Koshimizu are respectively equivalent to the plate 32 and the ring 30. The members 104 and 204 do not have the same disposition relative to the electrode 116 and 110 in Koshimizu that the plate 32 and the ring 30 have relative to the electrodes 24 and 22 in applicant's system. Furthermore, the members 104 and 204 in Koshimizu do not perform the same functions as the plate 32 and the ring 30 perform in applicants' system. On this basis, applicant

respectfully submits that Koshimizu is not a proper reference to show that the plate 32 and the ring 30 are known in the prior art.

Contrary to the position of the Examiner in the second full paragraph on page 5 of the Office Action dated 02/13/03, the susceptors 110 and 116 do not have the negative biases that are recited for the electrodes 24 and 22 in the claim of this application. Furthermore, the susceptors 110 and 116 are not parallel to the members 104 and 204. Specifically, applicant does not see how the process container 104 can be considered as equivalent to either the plate 32 or the ring 30, either in positioning or function. This is also true of the annular rail 204.

The Examiner has rejected claims 1-4, 7-9, 11, 14-16, 19-21, and 43-47 as anticipated by Koshimizu. However, the Examiner has cited Mountsier in support of Koshimizu to support his position that these claims are anticipated by Koshimizu. In support of his position, the Examiner has cited MPEP 2116.01. However, MPEP 2116.01 does not deal with anticipation. It deals with obviousness. Furthermore, it deals with obviousness in method claims. The Examiner's rejection should accordingly be considered as one of obviousness in view of Koshimizu when combined with Mountsier. This is particularly true since claims 1-21 do not deal with a method. It is also particularly true since the Examiner has had to use two (2) references to reject the claims and anticipation occurs only when a single reference is applied against the claims.

Even when considered on the basis of obviousness, claims 1-4, 7-9, 11, 14-16, 19-21, and 43-47 are allowable over the combination of Koshimizu and Mountsier because neither reference discloses the equivalent of electrodes 22 and 24. Neither reference

further discloses that the first electrode is biased to a first voltage and that the second electrode is biased to a second voltage lower than the first voltage. There is also no disclosure in either reference of the combination of first and second electrodes and first and second electrical conducting members, particularly since the relative dispositions and characteristics of the electrodes and the electrical conducting members are recited in the claims.

Claims 1-4, 7-9, 11, 14-16, 19-21, 43-47 and 50 are allowable over Koshimizu and Mountsier, individually and in combination, for the following additional reasons.

Claim 1

the second electrode and the wafer being disposed relative each other and to the ions of the inert gas, and the second electrode being constructed, to obtain a movement of the ions to the wafer at a low and controlled speed for an etching of the surface of the insulating layer by the ions at a low and controlled speed.

Claim 2

dependent from allowable claim 1;

the first member as recited in the claim;

the second member as recited in the claim;

the disposition of the first electrical field and the magnetic field as recited in the claim;

the disposition of the second electrical field and the magnetic field as recited in the claim;

the second electrode being contiguous to, but spaced from, the wafer.

Claim 3

dependent from allowable claim 1;

the bias on the second electrode being less than the bias on the first electrode.

Claim 4

dependent from allowable claim 1.

Claim 7

a first source of alternating voltage as recited in the claim;

a second source of alternating voltage as recited in the claim;

the wafer being disposed relative to the second electrode and relative to the ions of the inert gas in the enclosure to receive an etching of a low magnitude on the surface of the insulating layer by the ions of the inert gas in the enclosure.

Claim 8

dependent from allowable claim 7;

the operation of the first source of the alternating voltage as recited in the claim;

the operation of the second source of alternating voltage as recited in the claim;

the first electrode being disposed in contiguous, but spaced, relationship to the wafer.

Claim 9

dependent from allowable claim 7;

the disposition of a first electrical conductor as recited in the claim;

the disposition of a second electrical conductor as recited in the claim.

Claim 11

dependent from allowable claim 7;

the wafer being disposed in a spaced, but adjacent, relationship to the second electrode to create a first capacitor between the second electrode and the wafer and to create a second capacitor between the wafer and the ions of the inert gas in the enclosure.

Claim 14

a first source of an alternating voltage as recited in the claim;

a first electrode as recited in the claim;

a second source of voltage as recited in the claim;

a second electrode as recited in the claim;

the second electrode and the wafer providing a first capacitor of a high impedance, and the wafer and the ions in the enclosure providing a second capacitor of a low

impedance, in a circuit to produce a current of a low magnitude for etching the surface of the insulating layer in the wafer.

Claim 15

dependent from allowable claim 14;

the first capacitor including a dielectric of the molecules and ions of the inert gas and the second capacitor including a dielectric constituting the insulating layer.

Claim 16

dependent from claim 14;

disposition of a first electrically conductive member as recited in the claim;

disposition of a second electrically conductive member as recited in the claim.

Claim 19

dependent from allowable claim 14.

Claim 20

dependent from allowable claim 14;

disposition of a first electrically conductive member as recited in the claim;

disposition of a second electrically conductive member as recited in the claim;

disposition of a wafer and the floating potential on the wafer as recited in the claim.

Claim 21

first and second electrodes disposed in an enclosure and displaced from each other and from a wafer for producing electrical fields in the enclosure;

a first voltage source for producing a voltage of a high magnitude in the vicinity of the first electrode to obtain a production of a high electrical field in the enclosure;

a second voltage source for producing a voltage of a low magnitude in the vicinity of the second electrode to obtain a production of a low electrical field in the enclosure;

a supply of molecules of an inert gas for introduction into the enclosure to cooperate with the first and second electrodes and magnetic members in obtaining an ionization of the gas molecules in the enclosure by the electrical and magnetic fields in the enclosure and in obtaining a movement of the ions in the enclosure to the insulating layer in the wafer at a speed to obtain a smooth and uniform etching of the surface of the insulating layer at a low rate without any pits in the surface of the insulating layers.

Claim 43

dependent from allowable claim 21;

the second electrode provides the low electrical field in cooperation with the magnetic field for etching the surface of the insulating layer on the wafer to obtain the smooth and uniform etching on the surface of the insulating layer at the low rate without any pits in the surface of the insulating layer.

Claim 44

dependent from allowable claim 21;

the first voltage source applies an alternating voltage from the voltage source to the first electrode to produce a strong negative direct voltage in the vicinity of the first electrode;

the second voltage source applies an alternating voltage from the second source to the second electrode to produce a weak negative direct voltage in the vicinity of the second electrode.

Claim 45

dependent from allowable claim 21;

disposition of a first electrical conducting member as recited in the claim;

disposition of second electrical conducting member as recited in the claim.

Claim 46

dependent from allowable claim 45;

disposition of first and second electrical conducting members as recited in the claim.

Claim 47

dependent from allowable claim 46;

the first and second electrical conducting members are respectively disposed in a substantially parallel, but spaced, relationship to the first and second electrodes.

Claim 50

dependent from allowable claim 44;

first electrical conducting member and characteristics of the member as recited in the claim;

second electrical conducting member and characteristics of the member as recited in the claim.

5. Claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 and 51 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Koshimizu in view of Mountsier. Claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 and 51 are allowable over the combination of Koshimizu and Mountsier for certain important reasons which will be discussed in some detail below.

The Examiner has admitted on page 6 of the Office Action dated 02/13/2003 that Koshimizu does not disclose certain features recited in the claims. For example, the Examiner has admitted:

> "Koshimizu does not teach that the wafer and the first electrode define a series relationship between two capacitors , one having a high capacity impedance and the other having a low capacity impedance. Koshimizu does not provide apparatus to support an electrically floating substrate supported by a powered electrode."

The Examiner has then cited what he considers to be two (2) capacitors in Mountsier. Applicant does not see two (2) capacitors in what the Examiner has cited in Figures 5 and 6 of Mountsier. Even if there are two (2) capacitors in what the Examiner has cited in Mountsier, applicant does not see two (2) capacitors in series and applicant does not see one (1) capacitor with a high impedance and the other capacitor with a low impedance. Applicant further does not see how any capacitors in Mountsier limit the etching provided on the surface of a wafer. Applicant would accordingly appreciate it if the Examiner would specify in the next Office Action each of the two (2) capacitors, the conductive plates of each of the two (2) capacitors and the dielectric between the plates in each of the two (2) capacitors. Applicant would also appreciate it if the Examiner would show in Mountsier how any such capacitors limit the etching of a surface of a wafer.

Applicant notes that Mountsier discloses a wafer cooling device. A wafer cooling device does not provide a controlled deposition of material on a wafer. In view of this, applicant would appreciate it if the Examiner would indicate in the next Office Action where Mountsier specifies the components for providing an electrical field and a magnetic field substantially perpendicular to the electrical field for ionizing molecules of a gas and forming these ions to deposit material from a target on a wafer or substrate. More specifically, applicant would appreciate it if the Examiner would indicate in the next Office Action where Mountsier provides an anode, a target, an electrical field and a magnetic field.

As the Examiner will see from the discussion in the previous two (2) paragraphs, applicant does not believe that Mountsier is a pertinent reference against applicant's

claims. One reason is that Mountsier does not disclose deposition apparatus. A disclosure of a wafer cooling device as in Mountsier does not mean that Mountsier has disclosed apparatus for depositing a material from a target on a substrate. This would prevent Mountsier from being a pertinent reference against applicant's claims even if Mountsier disclosed two (2) capacitors in series. However, Mountsier does not disclose two (2) capacitors in series. Mountsier actually does not even disclose two capacitors. Certainly Mountsier does not disclose two (2) capacitors where one of these capacitors has plates defined by the equivalent of the electrode 22 and the electrically conductive deposition layers in the wafer 16 and has a dielectric defined by the gap between the equivalent of the electrode 22 and the wafer 16. Mountsier also does not disclose that the equivalent of the other of these capacitors has plates defined by the equivalent of the electrically conductive layers in the wafer 16 and the charge defined by argon ions in the vicinity of the electrode 22 and has a dielectric defined by the equivalent of the insulating layer 14.

In addition to the reasons discussed above, claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 and 51 are specifically allowable over the references for the following additional reasons:

Claim 5

dependent from allowable claim 4;

the wafer being at a floating potential;

there being first and second electrically conductive members respectfully adjacent, but spaced from, the first and second electrodes at a reference potential to provide for the creation of electrical fields respectively between the first electrode and the first electrically conductive member and between the second electrode and the second electrically conductive member.

Claim 6

dependent from allowable claim 2;

allowable for the same reasons as claim 5.

Claim 10

dependent from allowable claim 2;

the wafer being at a floating potential relative to the negative potentials on the first and second electrodes and relative to the reference potential.

Claim 12

dependent from allowable claim 10.

Claim 13

dependent from allowable claim 10;

disposition of a first electrical conductor as recited in the claim;

disposition of a second electrical conductor as recited in the claim;

the wafer being disposed in a spaced, but adjacent, relationship to the first electrode to create a first capacitor between the second electrode and the wafer and to create a second capacitor between the wafer and the ions of the inert gas in the enclosure.

Claim 17

dependent from allowable claim 14;

disposition of a first electrically conductive member as recited in the claim;

disposition of a second electrically conductive member as recited in the claim;

Claim 18

dependent from allowable claim 17.

Claim 20

dependent from allowable claim 14;

disposition of a first electrically conductive member as recited in the claim;

disposition of a second electrically conductive member as recited in the claim;

the wafer having a floating potential and being disposed between the first and second electrodes in closer proximity to the second electrode than to the first electrode.

Claim 48

dependent from allowable claim 48;

the wafer and the first electrode define a series relationship between two (2) capacitors, one having a high capacity impedance and the other having a low capacity impedance and the high capacity impedance limits the energy providing for the etching of the surface of the insulating layer in the wafer.

Claim 49

dependent from allowable claim 47;

the wafer and the first electrode define a series relationships between two (2) capacitors, one having a high capacity impedance and the other having a low capacity impedance and the high capacity impedance provides for the etching of the surface of the insulating layer in the wafer.

Claim 51

dependent from allowable claim 49;

the characteristics of the first alternating voltage as recited in the claim;

the characteristics of the second alternating voltage as recited in the claim;

a first electrical conducting member is disposed in a cooperative relationship with the first electrode to provide for the production of a high electrical field;

a second electrical conducting member is disposed in a cooperative relationship with the second electrode to provide for the production of the high electrical field.

6. In order for different prior art references to be combined to reject a claim, the references have to disclose or suggest the combination recited in the claim. AC Hospitality Systems, Inc. v Montefiore Hospital 1932 F.2d 1572, 221 USPQ 929 (Fed. Cir. 1984). As the Federal Circuit indicated in the ACS case at 732 F.2d 1577, 221 USPQ 933:

> "Obviousness cannot be established by combining the techniques of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under Section 103, teaching of references can be combined only if there is some suggestion or incentive to do so."

There is nothing in either of the references cited by the Examiner to support the combination of the references in the manner advanced by the Examiner. Furthermore, neither of the references discloses certain features recited in the claims. This has been discussed in detail above. The references cannot accordingly be combined to reject the claims.

7. Reconsideration and allowance of the application are respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification and the claims by this Amendment. The following pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

In light of the above amendments and remarks, applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Page 8, line 8:

The apparatus 10 includes an enclosure 20 which may be formed in part by an electrode 22, and electrode 24 displaced from, but preferably substantially parallel to, the electrode 22 and magnets 26 and 28 disposed in a transverse (preferably substantially perpendicular) relationship to the electrodes 22 and 24. The electrode 22 is disposed in a contiguous but spaced and substantially parallel relationship to the wafer 16 and is movable in position toward or away from the wafer, as indicated by a double-headed arrow 25. The spacing between the wafer 16 and the electrode 22 may illustratively be in the order of 0.1 – 2mm. A plate 30 extending from the magnet [26] 28 in a substantially parallel and adjacent, but spaced, relationship to the electrode 22 also defines the enclosure 20. A ring 32 extending from the magnet [28] 26 to a position spaced from, but adjacent to, the electrode 24 also defines in part the enclosure 20. The plate 30 and the ring 32 may be considered as electrical conductors. The ring 32 may be considered as one electrical conductor and the plate 32 may be considered as another electrical conductor.

Page 12, line 15:

As will be seen, the combination of the electrode 22 and the wafer 16 in Figure 5a is seen as a single electrode or plate in a capacitor 50 in Figure 5b. The other electrode or plate in the capacitor 50 is defined by the positive ions in the enclosure 20 at positions

adjacent the electrode 24. These positive ions are schematically illustrated by dots (.) at 51 in Figure 3. The dielectric between the plates of the capacitor 50 may be considered to be the insulating layer 14. The impedance of the capacitor 50 is accordingly relatively low because the [insulting] insulating layer 14 is relatively thin and because the dielectric constant of the insulating layer is lower than the dielectric constant of air or the dielectric constant of a vacuum.

IN THE CLAIMS

1. (Twice Amended) In combination for etching an insulating layer in a wafer to present a clean and fresh surface on the insulating layer for deposition,

a conduit for molecules of an inert gas,

a first electrode biased to a first voltage and spaced from the wafer,

a second electrode biased to a second voltage lower than the first voltage and spaced from the first electrode and the wafer and further spaced from the wafer than ~~the first electrode,~~

magnetic members providing a magnetic field,

the first electrode and the magnetic members being disposed relative to each other and to the molecules of the inert gas for ionizing the molecules of the inert gas, and

the second electrode and the wafer being disposed relative to each other and to the ions of the inert gas, and the second electrode being constructed, to obtain a

movement of the ions to the wafer at a low and controlled speed for an etching of the surface of the insulating layer by the ions at a low and controlled speed.

2. (Amended) In a combination as set forth in claim 1,

a first member disposed adjacent the first electrode for providing a reference potential different from the bias on the first electrode to create a first electrical field, and

a second member disposed adjacent the second electrode for providing the reference potential to create a second electrical field,

the first electrical field and the magnetic field being disposed relative to each other and to the molecules of the inert gas from the supply for ionizing the molecules of the inert gas,

the second electrical field and the magnetic field being disposed relative to each other and to the ions of the inert gas to obtain the movement of the ions to the wafer at the low and controlled speed,

the second electrode being contiguous to, but spaced from, the wafer.

3. (Amended) In a combination as set forth in claim 1,

a first source of alternating voltage for creating the bias on the first electrode, the bias on the first electrode being a negative direct voltage,

a second source of alternating voltage for creating the bias on the second electrode, the bias on the second electrode being a negative direct voltage,

the bias on the first electrode being less than the bias on the second electrode.

8. (Amended) In a combination as set forth in claim 7,

an opening in the enclosure for the flow of the molecules and ions of the inert gas from the enclosure,

the first source of the alternating voltage being operative to produce a direct voltage of the high magnitude and a negative polarity at the first electrode,

the second source of the alternating voltage being operative to produce a direct voltage of the low magnitude and a negative polarity at the second electrode,

the first electrode being disposed in contiguous, but spaced, relationship to the wafer.

13. (Twice Amended) In a combination as set forth in claim 10,

a first electrical conductor disposed in an adjacent, but spaced, relationship to the first electrode at a particular reference potential to produce a first electrical field between the first electrode and the first electrical conductor,

a second electrical conductor disposed in an adjacent [relationship], but spaced, relationship to the second electrode at the particular ~~reference potential~~ to produce a second electrical field between the second electrode and the second conductor,

the wafer being disposed in a spaced, but [adjacent] contiguous, relationship to the second electrode to create a first capacitor between the second electrode and the wafer and to create a second capacitor between the wafer and the ions of the inert gas in the enclosure.

15. (Amended) In a combination as set forth in claim 14,

the first capacitor [providing] including a dielectric of the molecules and ions of the inert gas and the second capacitor [providing] including a dielectric constituting the insulating layer.

16. (Amended) In a combination as set forth in claim 14,

a first electrically conductive member disposed in an adjacent but spaced relationship to the first electrode and having a reference potential to provide an electrical field between the first electrode and the first electrically conductive member, and

a second electrically conductive member disposed in an adjacent but spaced relationship to the second electrode and having the reference potential to provide an electrical field between the second electrode and the second electrically conductive member.

21. (Twice Amended) In combination for etching an insulating layer in a wafer to present clean and fresh surfaces on the insulating layer for deposition,

an enclosure [defined by first and second electrodes displaced from each other and from the wafer for producing electrical fields in the enclosure, and further defined by magnetic members for producing a magnetic field in the enclosure,]

first and second electrodes disposed in the enclosure and displaced from each other and from the wafer for producing electrical fields in the enclosure, and

magnetic members disposed in the enclosure for producing a magnetic field in the enclosure in a direction transverse to the electrical field,

a first voltage source for producing a voltage of a high magnitude in the vicinity of the first electrode to obtain a production of a high electrical field in the enclosure,

a second voltage source for producing a voltage of a low magnitude in the vicinity of the second electrode to obtain a production of a low electrical field in the enclosure, and

a supply of molecules of an inert gas for introduction into the enclosure to cooperate with the first and second electrodes and the [magnets] magnetic members in obtaining an ionization of the gas molecules in the enclosure by the electrical and magnetic fields in the enclosure and in obtaining a movement of the ions in the enclosure to the insulating layer in the wafer at a speed to obtain a smooth and uniform etching of the surface of the insulating layer at a low rate without any pits in the surface of the insulating layer.

25. (Amended) A method as set forth in claim 22 wherein

the wafer is disposed in the relatively weak electrical field and wherein

an electrode providing the relatively weak electrical field is spaced from, but disposed relatively close to, the wafer to cooperate with the wafer in providing a high impedance in the capacitor and a circuit including the capacitor for attracting the ions in the weak electrical field to the wafer to etch the surface of the insulating layer on the wafer without pitting the insulating layer.

26. (Twice Amended) A method as set forth in claim 22 wherein

the capacitor constitutes a first capacitor and wherein

the relatively weak electrical field is defined by the first capacitor and a second capacitor in a series circuit and wherein

the first capacitor is defined by plates constituting an electrode and the wafer and in which the plates of the first capacitor are separated by a space in which molecules and ions of the inert gas are disposed to define the insulator for the first capacitor and to provide the first capacitor with the high impedance and wherein

a second capacitor is defined by plates constituting the wafer and the ions of the inert gas in the enclosure and wherein the plates of the second capacitor are separated by the insulating layer in the wafer to define the insulator of the second capacitor and to provide the second capacitor with a relatively low impedance in comparison to the high impedance of the first capacitor.

28. (Twice Amended) A method as set forth in claim 26 wherein

the wafer is disposed in the relatively weak electrical field and wherein

the molecules of the inert gas are passed through the enclosure initially through positions in the relatively strong electrical field to obtain an ionization of molecules of the inert gas and subsequently through positions in the relatively weak electrical field to facilitate a substantially uniform etching of the surface of the insulating layer on the wafer by the ions and wherein

the wafer is disposed in the relatively weak electrical field and wherein

an electrode providing the relatively weak field is spaced from, but disposed relatively close to, the wafer to cooperate with the wafer in providing a high impedance in the first capacitor and a circuit including the second capacitor for attracting

the ions in the weak electrical field to the wafer to etch the surface of the insulating layer on the wafer without pitting the insulating layer.

29. (Twice Amended) A method as set forth in claim 26 wherein

the capacitor constitutes a first capacitor and wherein

the first capacitor and a second capacitor are in series and wherein

the first capacitor is defined by plates constituting an electrode and the wafer and wherein

the plates of the first capacitor are separated by a space in which molecules and ions of the inert gas are disposed to define the insulator for the capacitor and to provide the high impedance and wherein

the second capacitor is defined by plates constituting the wafer and the ions of the inert gas in the enclosure and wherein the plates of the second capacitor are separated by the insulating layer in the wafer to define the insulator of the second capacitor and to provide a relatively low impedance in comparison to the high impedance of the first capacitor and wherein

the relatively strong electrical field is provided by a first electrode and a first alternating voltage providing a relatively high negative bias on the first electrode and wherein

the relatively weak electrical field is provided by a second electrode and by a second alternating voltage providing a relatively low negative bias on the second electrode.

42. (Twice Amended) A method as set forth in claim 37 including the steps of:

introducing an alternating voltage of a first particular magnitude to the first electrode to produce a strong negative DC bias on the first electrode for the creation of the strong electrical field,

introducing an alternating voltage of a second particular magnitude less than the first particular magnitude to the second electrode to produce a weak negative DC bias on the second electrode for the creation of the weak electrical field, and

providing a high impedance between the second electrode and the wafer and a low impedance between the wafer and the charged particles near the wafer to produce a transfer of charged particles with limited energy to the surface of the insulating layer and the walls of the socket in the insulating layer and to provide the weak and controlled etching of the surface of the insulating layer and the walls of the socket with a substantially uniform thickness of material from the insulating layer and the wall of the socket without pitting the surface of the insulating layer or the walls of the socket.

43. (Twice Amended) ~~In a combination as set forth in claim 21 wherein,~~

the first electrode provides the high electrical field in cooperation with the magnetic field for producing an ionization of molecules of [an] the inert gas in the enclosure and wherein

the second electrode provides the low electrical field in cooperation with the magnetic field for etching the surface of the insulating layer on the wafer to obtain the smooth and uniform etching on the surface of the insulating layer at the low rate without any pits in the surface of the insulating layer.

44. (Amended) In a combination as set forth in claim 21 wherein

the first voltage source applies an alternating voltage [applied] from the voltage source to the first electrode to produce a strong negative direct voltage in the vicinity of the first electrode and wherein

[wherein] the second voltage source applies an alternating voltage from the second voltage source to the second electrode to produce a weak negative direct voltage in the vicinity of the second electrode.

45. (Amended) In a combination [a] as set forth in claim 21 wherein

a first electrical conducting member is disposed in a cooperative relationship with the first electrode to provide for the production of the high electrical field and wherein

a second electrical conducting member is disposed in a cooperative relationship with the second electrode to provide for the production of the low electrical field.

46. (Amended) ~~In a combination as set forth in claim 45 wherein[,]~~

the first and second electrodes are substantially parallel to the wafer and wherein

the first and second electrical conducting members are substantially parallel to the first and second electrodes.

49. (Amended) In a combination as set forth in claim 47 wherein[,]

the wafer and the first electrode define a series relationship between two (2) capacitors, one having a high capacity impedance and the other having a low capacity

impedance and wherein the high capacity impedance limits the energy providing for the etching of the surface of the insulating layer in the wafer.

50. (Amended) In a combination a set forth in claim 44 wherein

a first electrical conducting member is disposed in a cooperative relationship with the first electrode to provide for the production of the high electrical field and wherein

a second electrical conducting member is disposed in a cooperative relationship with the second electrode to provide for the production of the low electrical field.

51. (Amended) In a combination as set forth in claim 49 wherein

the first voltage source applies an alternating voltage from the first voltage source to the first electrode to produce a strong negative direct voltage in the vicinity of the first electrode and wherein

the second voltage source applies an alternating voltage from the second ~~voltage source to the second electrode to produce a weak negative direct voltage in the~~ vicinity of the second electrode and wherein

a first electrical conducting member is disposed in a cooperative relationship with the first electrode to provide for the production of the [high] strong electrical field and wherein

a second electrical conducting member is disposed in cooperative relationship with the second electrode to provide for the production of the [low] weak electrical field.